UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,439	01/31/2006	Eckhard Wolfgang	1454.1671	3860

21171 7590 04/22/2008

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
04/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,439	WOLFGANG ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-21,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-21,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 30, 2008, has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 11, 12 and 21** are rejected under 35 U.S.C. 102(e) as being anticipated by **Akram et al. (US 2004/0036157, previously cited, hereinafter Akram)**.

With respect to **claim 11, Akram** teaches a circuit device provided on a substrate **(FIGs. 4A-4F)** and comprising:

a single active semiconductor component **(12, FIG. 4A; ¶ [0034]-[0037], [0050])** arranged on the substrate **(¶ [0049]: "wafer")** and having an outer electrical contact surface **(top surface of contact 16, FIG. 4A; ¶ [0037], [0050])**; and

at least one electrical connection line **(34, FIG. 4B; ¶ [0051])** on the substrate to contact with the outer electrical contact surface **(top surface of 16)** of the single active semiconductor component **(12)**,

wherein the electrical connection line **(34, FIG. 4E; ¶ [0054])** is part of at least one discrete passive electrical component **(32)** arranged on the substrate,

wherein the electrical connection line **(34; ¶ [0051])** contacts the outer electrical contact surface **(top surface of 16, FIG. 4B)** at an electrical contact **(16)**, the electrical contact faces away from the substrate **(12)**; and

a layer of electrically insulating film **(18, FIG. 4A; ¶ [0050])** is laminated on the single active semiconductor component **(12)** and the substrate **(12)** in such a way that the electrical contact **(16)** is exposed **(FIG. 4A; ¶ [0050])**.

With respect to **claim 12,** which is dependent on claim 11, **Akram** teaches wherein the discrete passive electrical component is a capacitor **(32, FIG. 4E; ¶ [0054])** and the electrical connection line **(34)** is an electrode of the capacitor **(FIG. 4E)**.

With respect to **claim 21, Akram** teaches wherein a method for producing a circuit device **(Figs. 4A-4F; ¶ [0049]-[0058])**, comprising:

producing a single active semiconductor component **(12, FIG. 4A; [0037]-[0034], [0050])** on a substrate **(¶ [0049]: "wafer")**, the single active semiconductor component having an outer electrical contact surface **(top surface of 16, ¶ [0050])** facing away from the substrate; and

producing an electrical connection line **(34, FIG. 4B; ¶ [0051])** that contacts the outer electrical contact surface **(top surface of 16)** of the single active semiconductor component **(12)**, the electrical connection line **(34; ¶ [0051])** is part of a discrete passive electrical component **(32; ¶ [0054])**, wherein the electrical connection line **(34; ¶ [0041])** contacts the outer electrical contact surface **(top surface of 16)** at an electrical contact **(16)**, such that the electrical contact faces away from the substrate; and

laminating a layer of electrically insulating film **(18, FIG. 4A; ¶ [0050])** onto the single active semiconductor component **(12)** and the substrate **(¶ [0049]: wafer)** in such a way that the electrical contact **(16)** is exposed **(FIG. 4A; ¶ [0050])**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 11-15, 18 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chu et al. (6,365,498; as previously cited)** in view of **Kung et al. (US 6,197,613; as previously cited)**.

With respect to **claim 11 and 24, Chu** teaches a circuit device provided on a substrate **(22, Figs. 2A-2F and 3)** and comprising:

a semiconductor component **(integrated circuits with bond pad 24; col. 1: lns. 7-13, col. 2: lns. 61-65)** arranged on the substrate **(wafer 22, Fig. 2A)** and having an

outer electrical contact surface **(top surface 34 of bond pad 24; col. 5: lns. 45-60)**; and

at least one electrical connection line **(30, Fig. 2A; 40, Fig. 2F; col. 5: lns. 55-57; col. 6: lns. 5-15)** on the substrate **(12)** to contact with the outer electrical contact surface **(34)** of the semiconductor component **(integrated circuits with bond pad 24)**,

wherein the electrical connection line **(30, 40)** is part of at least one discrete passive electrical component **(36, 38, 48; Figs. 2D, 2E and 3; col. 5: lns. 63-67; col. 6: lns. 5-21)** arranged on the substrate **(22)**,

wherein the electrical connection line **(30, 40)** contacts the outer electrical contact surface **(34, Fig. 2A)** at an electrical contact **(34)**, the electrical contact faces away from the substrate **(22)**; and

a layer of electrically insulating film **(28, Fig. 2A)** is laminated onto a least two surfaces of the semiconductor component **(integrated circuits with bond pad 24)** and the substrate **(wafer 22)** in such a way that the electrical contact **(34)** is exposed **(Fig. 2A)**.

Thus, **Chu** teaches all the limitations of the claim with the exception of explicitly disclosing wherein the semiconductor component is a single active semiconductor component arranged on the substrate.

However, **Kung** discloses an IC device **(10, FIG. 1A)** wherein single active semiconductor components are arranged on the substrate **(12)** to form integrated circuits **(col. 2: lns. 5-19)**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the integrated circuits of **Chu** with

single active semiconductor components, as taught by **Kung**, because active components, such as transistors, on a semiconductor substrate is well known and conventionally used in semiconductor devices, such as memory components.

With respect to **claim 12,** which is dependent on claim 11, **Chu** teaches wherein the discrete passive electrical component is a capacitor **(48, Fig. 3; col. 6: lns. 5-21)** and the electrical connection line **(40)** is an electrode of the capacitor **(48)**.

With respect to **claim 13,** which is dependent on claim 11, **Chu** teaches wherein the discrete passive electrical component is a coil **(36, Fig. 2E)**, and the electrical connection line **(30; col. 5: lns. 57-67)** is a winding of the coil **(col. 4: lns. 45-48)**.

With respect to **claim 14,** which is dependent on claim 11, **Chu** teaches wherein the discrete passive electrical component is an electrical resistor **(36, 38, Figs. 2C and 2D)**, and the electrical connection line **(30)** is a wire resistor **(col. 5: lns. 57-67)**.

With respect to **claim 15,** which is dependent on claim 11, **Chu** teaches wherein the discrete passive electrical component is a part of a sensor of a physical variable **(the electrical wire resistors 36 and 38, formed from connection line 30 can act as temperature sensors)**.

With respect to **claim 18,** which is dependent on claim 14, **Chu** teaches wherein the discrete passive electrical component is a part of a sensor of a physical variable **(the electrical wire resistors 36 and 38, formed from connection line 30, can act as temperature sensors)**.

4. **Claims 16, 17, 19 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chu ('498, cited above) and Kung ('613, cited above)**, as applied above to claims 11 and 14, respectively, and further in view of **Iseki et al. (US 2002/0036345, as previously cited)**.

With respect to **claims 16,17, 19 and 20 Chu and Kung** discloses all the limitations of the claim, as set forth above in claims 11 and 14, respectively, with the exception of disclosing: wherein the semiconductor component is a power semiconductor component, selected from the group consisting of MOSFETs, IGBTs, and bipolar transistors.

However, **Iseki** teaches that an integrated circuit device may comprise of bipolar transistors, IGBTs or power MOSFETs **(pg. 10: [0108])**, which are used for high frequency or high power applications.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to form the IC device of **Chu and Kung,** with power semiconductor components such as IGBTs and MOSFETs, as taught by **Iseki,** because such power transistors provide high frequency and high power applications.

5. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Akram ('157, cited above)**, as applied to claim 21, and in view of **Kung ('613, cited above)**.

With respect to claim 23, **Akram** teaches all the limitations of the claim, as set forth above in claim 21, including wherein the layer of electrically insulating material **(18, FIG. 4A)** is applied, and the electrical contact **(16)** is exposed by opening a window **(68)**

in the electrically insulating material **(¶ [0050])**. Thus, Akram discloses all the limitations of the claim with the exception of explicitly disclosing that the insulating material is applied first, and then the window in the insulating material is opened. However, Kung discloses a method wherein the electrically insulating material **(20, FIG. 1A)** is applied first, and then an electrical contact **(14)** is exposed by opening a window **(22)** in the electrically insulating film **(col. 2: lns. 11-14)**. Therefore, it would have been obvious to one of ordinary skill in the art, to incorporate the teaching of Kung into the method of Akram, to apply an insulating film first, and then expose the contact by opening a window using a photolithography process, because such photolithography techniques are well known, and typically used in the semiconductor art to allow connection to bond pads **(FIG. 1A, col. 2: lns. 5-14)**.

Furthermore, note that selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results; In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930). MPEP 2144.04.

Response to Arguments

6. Applicant's arguments with respect to claims 11-21 and 23 have been considered but are not persuasive.

With respect to claim 1 and the Akram reference, Applicant argues "Akram does not discuss or suggest a single active semiconductor component arranged on the substrate and having an outer electrical contact surface."

The argument is not persuasive. In paragraph [0049], Akram teaches a single active semiconductor component (semiconductor die 12) is contained on a semiconductor substrate (semiconductor wafer). Regarding the "outer electrical contact surface," Akram states that the "die 12 includes die contacts 16, such as bond pads embedded within an electrically insulating passivation layer 18 (¶ [0037])."

Applicant also argues:

> "As to the Examiner's assertion that the die contact 16 is the outer electrical contact surface of the integrated circuit 24, the Examiner is implicitly alleging that the combination of the integrated circuit 24, the internal conductor 22 and the die contact 16 correspond with a semiconductor component. The Applicants respectfully disagree. Claim 11 recites 'a single active semiconductor component [emphasis added].' However, the die contact 16 having an outer electrical contact surface, in addition to the internal conductor 22 and the integrated circuit 24 are not altogether a single active semiconductor component."

The argument is not persuasive because Akram teaches that the semiconductor component (semiconductor die 12) includes integrated circuits 24, internal conductors 22 and die contacts 16 (¶ [0050]). Furthermore, in paragraph [0034], Akram states that: "As used herein, the term 'semiconductor component' refers to an electronic element that includes a semiconductor die."

With respect to claims 1 and 21, and the Akram reference, Applicant argues:

> "Further, Akram does not discuss or suggest that a layer of electrically insulating film is laminated onto the semiconductor component and the substrate in such a way that the electrical contact is exposed. The passivation layer 18, which is located on portions of die contact 16, is not laminated onto the integrated circuit 24 in such a way as to expose the die contact 16, alleged by the Examiner to correspond with the semiconductor component."

The argument is not persuasive because Akram discloses that a layer of electrically insulating film 18 is laminated onto the semiconductor component 12 and the

substrate (¶ [0049]: "wafer") in such a way that electrical contact 16 is exposed (FIG. 4A; ¶ [0050]). Furthermore, the term laminate is defined on page 671 of *Webster's Ninth New Collegiate Dictionary* as: "to unite layers of material by an adhesive or other means." Also note, claim 1 is drawn to structure, and thus, any process limitations are not given patentable weight. A "product by process" claim is directed to the product per se, no matter how actually made; *In re Thorpe et al.,* 227 USPQ 964, (CAFC, 1985).

With respect to claim 1, and the Chu and Kung references, Applicant argues:

> "Chu discusses an IC device 20 which includes a substrate 22, a passivation layer 28, a bond pad 24, and a copper trace 40 in communication with the bond pad 24. As conceded by the Examiner, Chu does not suggest that a single active semiconductor component is arranged on the substrate 22 and does not suggest that the component has an outer electrical contact surface. The Examiner alleges that Kung makes up for the deficiencies in Chu. The Applicants respectfully disagree."
>
> "Kung discusses an IC device 10 that includes a bond pad 14 on a substrate 12, a passivation layer 20 and an adhesion/diffusion barrier layer 30. Kung does not discuss or suggest a single active semiconductor component arranged on the substrate 12 and having an outer electrical contact surface for communication with an electrical connection line. Kung discusses specifically that the semiconductor structure 10 is built on a silicon substrate 12 with active devices built therein. The active devices in Kung are built in substrate 12 and not on the substrate 12. Further, the bond pad 14 is not a single active semiconductor component that has an outer electrical contact surface for communication with an electrical connection line. The bond pad 14 is designed to be in contact only with a barrier layer, and does not provide an outer electrical contact surface."

The arguments are not persuasive. First, the Office did not concede that Chu "does not suggest that the component has an outer electrical contact surface," as stated by the Applicant. In the Final Rejection mailed on July 30, 2007, the Office stated that "Chu teaches all the limitations of the claim with the exception of disclosing wherein a single active semiconductor component is arranged on the substrate (page 6 of the Office Action)." Regarding the limitation of "single active semiconductor component

arranged on the substrate," Kung discloses that a conventional semiconductor structure 10 is built on a silicon substrate 12 with active devices built therein (col. 2: lns. 5-7). Applicant's argument that "the active devices in Kung are built in substrate 12 and not on the substrate 12," is not persuasive because the fact that the active devices are "built therein," implies that a portion of substrate is below the active devices, and thus, Kung implicitly teaches wherein active devices are formed on a portion of the substrate. Furthermore, note that the claim does not require the semiconductor component to be formed on or over a top surface of the substrate. Also note, that although Kung is not relied upon to teach "an outer electrical contact surface," as discussed above, Applicant's argument that bond pad 14 does not provide an outer electrical contact surface is incorrect. Kung clearly states that "a window 22 is opened by a photolithography process to allow electrical connection to be made to the bond pad 14 (col. 2: lns. 12-14)." Regarding the Applicant's argument against the motivation to combine the references, note that only Kung's teaching of "a single active semiconductor component formed on a substrate," is being incorporated into Chu's device, since such a limitation is well known and conventional in the art. Kung states that structure 10 is a conventional semiconductor structure (col. 2: lns. 5-7). Furthermore, FIGs. 1A-1B and 3 of **US Patent 6,623,985**, shows that forming active devices, such as transistors, on a substrate is well known and typical in semiconductor components, such as memory cells. Applicant has not provided any evidence or rationale to show that such a limitation is not well known or conventional.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X Cao/
Primary Examiner, Art Unit 2814